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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,186	01/14/2004	Jimmies Earl DeWitt JR.	AUS920030540US1	4157

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EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,186	DEWITT ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Notice to Applicants

This application, previously assigned to and examined by Ex. Justin King, is now assigned to Ex. Khanh Dang. Any contact should be directed to Ex. Khanh Dang, whose contact information is provided at the end of this Office Action.

The following is a reproduction of the Non-Final Office Action issued by Ex. King on 5/18/2006. Applicants' arguments including arguments relating to any new limitation added by the amendment filed 8/16/2006 will be fully and specifically addressed under "Response to Argument."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8-12, and 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Levine et al. (U.S. Patent No. 5,691,920)

Referring to claim 1: Levine discloses a performance-monitoring unit (Abstract) and one or more hardware counters (column 10, lines 58-59) located within the performance-monitoring unit (figure 4, structures 50 and 51). Levine discloses a variety

of operations of the performance-monitoring unit (column 10, lines 34-56); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Furthermore, Levine disclosed two separate counters for selected events (figure 6A, column 8, lines 57-60). Hence, the claim is anticipated by Levine.

Referring to claims 2-3: Since the nature of an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine; thus, any events been monitored during the interrupt is during a state of the interrupt.

Referring to claim 4: Levine discloses monitoring instruction execution and storage control (column 1, lines 65), which are the claimed multiple types of events.

Referring to claim 5: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 6: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claims 8-10: The rejections for the claims 1-3 apply; furthermore, Levine discloses that to effectively evaluate the flow of the instructions through the

processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Since Levine discloses that it is preferred to examine all stages, Levine implicitly discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt.

Referring to claim 11: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claim 12: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 13: Levine discloses one or more hardware counters (column 10, lines 58-59).

Referring to claim 14: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, and the instructions within specific addresses are a selected interrupt handling routine, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 16: The rejections for the claims 1-3 apply; furthermore, Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Since Levine discloses that it is preferred to examine all stages, Levine discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt.

Referring to claim 17: The nature of an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine.

Referring to claim 18: Levine discloses clock cycles (column 1, lines 66-67) and cache misses (column 14, line 9).

Referring to claim 19: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 20: Levine discloses one or more hardware counters (column 10, lines 58-59).

Referring to claim 21: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, and the instructions within specific addresses are a selected interrupt handling routine, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6, 8-14, and 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Levine.

Referring to claim 1: The admitted prior art discloses a performance-monitoring unit (Specification, page 3, last paragraph, line 6) and one or more hardware counters (Specification, page 3, last paragraph, lines 1-2) located within the performance-monitoring unit. The admitted prior art does not disclose that the one or more hardware counters count the occurrence of events during an interrupt of a selected type.

Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-39); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck. Hence, it would have been obvious to one having ordinary skill in the computer art at the time

Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck.

Referring to claim 2: Since an interrupt process comprises of an interrupt request, interrupt request acceptance, passing the control to the interrupt handler, and interrupt service routine (Specification, page 4, 2nd paragraph, lines 3-11); thus, any events been monitored during the interrupt is during a state of the interrupt.

Referring to claim 3: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 4: The admitted prior art discloses monitoring multiple types of events (Specification, page 3, last paragraph, lines 3-4, page 4, 1st paragraph, lines 5-7).

Referring to claim 5: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 6: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claims 8-9: The rejections for the claims 1-3 apply; the admitted prior art does not explicitly discloses counting at least one event for either a selected state of

the interrupt or each state of the interrupt. Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Levine's examination on all stages are the claimed counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine teaches one on how to locate the performance bottleneck by tracing the processing through all stages.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one on how to locate the performance bottleneck for improve the system performance.

Referring to claim 10: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 11: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claim 12: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 13: The admitted prior art discloses one or more hardware counters (Specification, page 3, last paragraph, lines 1-2).

Referring to claim 14: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or

more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Referring to claim 16: The rejections for the claims 1-3 apply; the admitted prior art does not explicitly discloses counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine discloses that to effectively evaluate the flow of the instructions through the processor's pipeline, all stages are *preferably* examined simultaneously (column 14, lines 63-65). Levine's examination on all stages are the claimed counting at least one event for either a selected state of the interrupt or each state of the interrupt. Levine teaches one on how to locate the performance bottleneck by tracing the processing through all stages.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teaching onto the admitted prior art because Levine teaches one on how to locate the performance bottleneck for improve the system performance.

Referring to claim 17: The admitted prior art discloses that the interrupt includes states of accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return (Specification, page 4, 2nd paragraph, lines 3-11).

Referring to claim 18: The admitted prior art discloses counting clock cycles and cache misses (Specification, page 3, last paragraph, lines 3-4).

Referring to claim 19: Levine discloses monitoring multiple types of events during the stall, which is the claimed counting multiple types of events for the same state.

Referring to claim 20: The admitted prior art discloses one or more hardware counters (Specification, page 3, last paragraph, lines 1-2).

Referring to claim 21: Since Levine discloses monitoring these interrupts based on the particular instruction addresses, Levine's performance-monitoring unit's one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

Claims 7, 15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Levine in view of previously cited "Computer System Architecture" by Morris Mano or as being unpatentable over the admitted prior art in view of Levine and Mano.

Referring to claims 7, 15, and 22: The disclosures of the admitted prior art and Levine are stated above. As stated above, Levine discloses monitoring the particular interrupt according to the instructions address, and Levine discloses two separate counters for event selections (figure 6A, column 8, lines 57-60); thus, Levine discloses the hardware counters counting events separately. But neither explicitly discloses a second interrupt interrupts a first interrupt.

Mano, as a popular academic textbook, discloses managing interrupt according to its priority (pages 434-435). Mano discloses that a higher priority interrupt can interrupt an in-process lower priority interrupt (page 435, 2nd paragraph). Mano teaches one to manage the limited system resources by prioritizing interrupt. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt Mano's

teaching onto the admitted prior art and Levine because Mano teaches one to manage the limited system resources by prioritizing interrupt.

Response to Arguments

Applicants' arguments filed 8/16/2006 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. As a matter of fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.*, 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The 102 Rejection:

With regard to claim 1, Applicants argued that:

> Applicants respectfully submit that Levine does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Levine does not teach or suggest "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events during processing of an interrupt of a selected type".

Contrary to Applicants' argument, Levine, as a matter of fact, discloses "one or more hardware counter located within the performance monitoring unit." As clearly shown in Fig. 4, which is reproduced below;

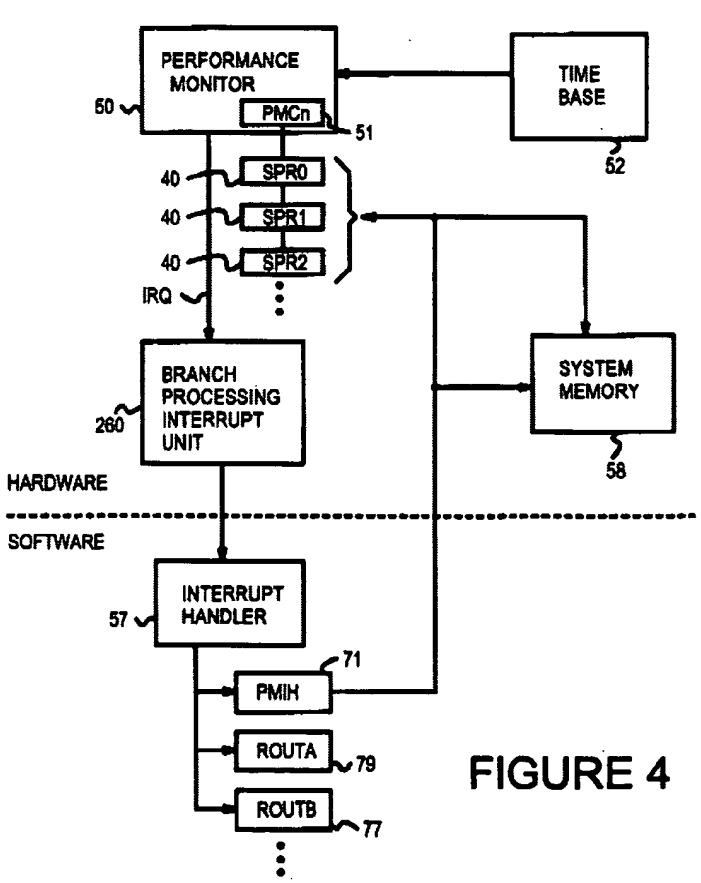

FIGURE 4

one or more hardware counters PMCn 51 are located within the performance monitor 50. As also disclosed by Levine, the performance monitor 50 is intended to provide detailed information with significant granularity concerning the utilization of PowerPC instruction execution and storage control. Generally, the performance monitor 50 includes counters 51 for counting processor/storage related events. See at least column 8, lines 33-41. Levine further discloses that when the performance monitor 50 receives the notification from time base 52 to indicate that it should record "sample data", an interrupt signal is output to a branch processing unit 20. Such interrupt type is called "a performance monitoring interrupt" occurred at a selectable point in the processing. As in any type of interrupt, the performance monitor interrupt causes the processor to save its state of execution, and begin execution of an interrupt handler (also known as interrupt service routine). It is clear that in this case, during servicing or processing the performance mnitor interrupt, the service routine for the performance monitring interrupt monitors performance by counting the number of related events. See at least column 9, line 63 to column 10, line 32.

In response to Applicants with regard to claim 2, the counters count the occurrence of events during the interrupt service routine, which is a "state" of the performance monitor interrupt.

In response to Applicants' argument regarding claim 4, it is clear from discussion above and also from column 17, line 50 to column 19, line 42, that multiple events are counted during servicing or processing of the performance monitor interrupt.

In response to Applicants' argument regarding claims 8 and 16, see discussion above. Further, it is clear that the states of the performance monitor interrupt include at least the state wherein an interrupt signal is generated, and a state wherein the interrupt is serviced or processed. As discussed above, during servicing or processing the performance monitor interrupt, multiple events are counted by hardware counters located inside the performance monitor unit 50.

The 103 Rejection:

With regard to claims 1-6, 8-14, and 16-21, Applicants argued that:

> Applicants submit that the Examiner has not established a *prima facie* case of obviousness with respect to the claims. As discussed in detail above, Levine does not disclose or suggest "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events during processing of an interrupt of a selected type" as recited in claim 1. The admitted prior art does not supply the deficiencies in Levine as discussed in detail above, and claims 1-6, 8-14 and 16-21 are, therefore, not obvious in view of the admitted prior art and Levine, and are allowable thereover in their present form. Applicants believe that only Applicants' disclosure teaches the combination asserted by the Examiner, and that the Examiner is using hindsight in attempting to combine the admitted prior art with Levine in an effort to achieve the present invention.
>
> Therefore, the rejection of claims 1-6, 8-14 and 16-21 under 35 U.S.C. § 103 has been overcome.

Contrary to Applicants' argument, at the outset, it is noted that In response to applicant's argument, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one

or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). As discussed above, "one or more hardware counter located within the performance monitoring unit." As clearly shown in Fig. 4, which is reproduced below;

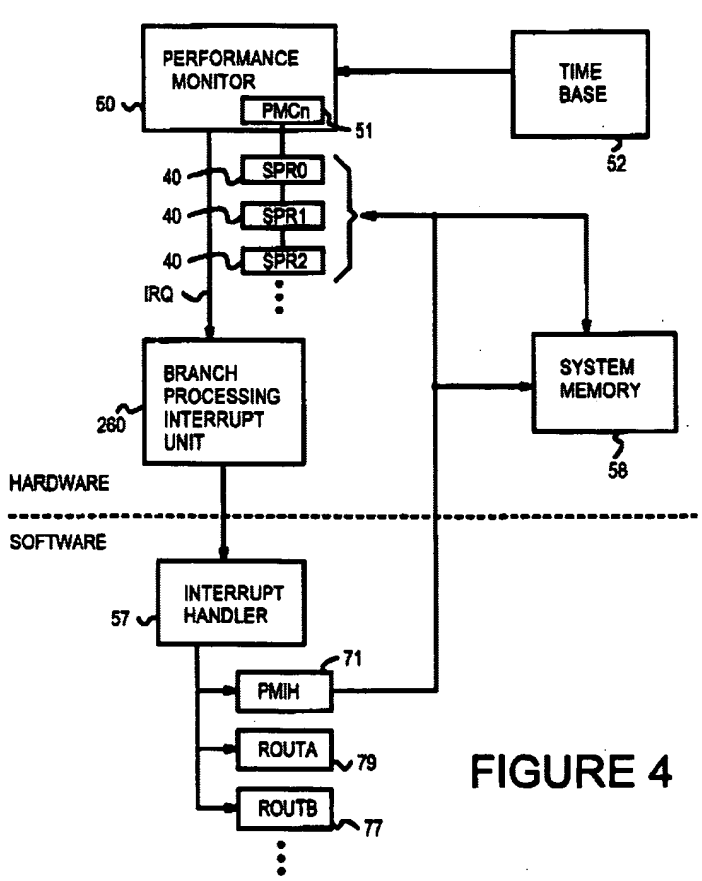

FIGURE 4

one or more hardware counters PMCn 51 are located within the performance monitor 50. As also disclosed by Levine, the performance monitor 50 is intended to provide detailed information with significant granularity concerning the utilization of PowerPC instruction execution and storage control. Generally, the performance monitor 50 includes counters 51 for counting processor/storage related events. See at least

column 8, lines 33-41. Levine further discloses that when the performance monitor 50 receives the notification from time base 52 to indicate that it should record "sample data", an interrupt signal is output to a branch processing unit 20. Such interrupt type is called "a performance monitoring interrupt" occurred at a selectable point in the processing. As in any type of interrupt, the performance monitor interrupt causes the processor to save its state of execution, and begin execution of an interrupt handler (also known as interrupt service routine). It is clear that in this case, during servicing or processing the performance mnitor interrupt, the service routine for the performance monitring interrupt monitors performance by counting the number of related events. See at least column 9, line 63 to column 10, line 32.

Further, as clearly stated in the 103 Rejection, the benefits and advantages are readily realized by employing the performance monitor taught by Levine. As set forth in MPEP Section 2144, "the strongest rationale for combining references is a recognition, expressly or impliedly in the prior art or drawn from a convincing line of reasoning based on established scientific principles or legal precedent, that some advantage or expected beneficial result would have been produced by their combination. *In re Sernaker*, 702 F.2d 989, 994-95, 217 USPQ 1, 5-6 (Fed. Cir. 1983)." In the instant case, the advantage or expected beneficial result, which would have been produced by the combination, is a significant improvement in system performance, obtained by indicating and resolving performance bottlenecks.

With regard to claims 7, 15, and 22, Applicants argued that:

> Mono is cited as disclosing monitoring interrupts according to their priority. Mono does not, however, disclose counting events separately that occur "during the processing of the interrupt of the selected type and during processing of the second interrupt" that interrupts the interrupt of the selected type as recited in claim 7. Further, Mano does not supply the deficiencies in Levine or in Levine and admitted prior art. Claim 7 and corresponding claims 15 and 22, accordingly, are allowable in their present form, and it is respectfully requested that the Examiner so find.

Contrary to Applicants' argument, at the outset, it is noted that Applicants cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

As clearly discussed above, in Levine, multiples events are counted separately by hardware counters during servicing or processing of a performance monitor interrupt. Further, the performance monitor interrupt is occurred at a selectable point in the processing. Depending on the number of "sample data" requests, multiple performance monitor interrupts can be generated, and events are separately counted during servicing or processing of a respective performance monitor interrupt.

Relevant Art

US Patent No 6,772,322 to Merchant et al. is cited as relevant art.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday-Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Khanh Dang
Primary Examiner